from July 2004 *High Frequency Electronics*

Load Network Design Techniques for Class E RF and Microwave Amplifiers

By Andrei Grebennikov
M/A-COM Eurotec

The output network of a class E amplifier must provide impedance matching at the fundamental frequency and adequate rejection of harmonic frequencies, while handling DC power to the device

The switched-mode second-order Class E amplifier configuration can be designed with a generalized load network that includes the shunt capacitance, series bondwire inductance, finite DC feed inductance and series L_0C_0 circuit. Based on theoretical analysis, this article examines the required voltage and current waveforms, and circuit parameters are determined for particular circuits corresponding to: Class E with shunt capacitance, even harmonic Class E, parallel-circuit Class E, and Class E with quarter wave transmission line. The effect of the device output bondwire inductance on the optimum load network parameters is shown. The operating power gain achieved with the parallel-circuit Class E power amplifier is evaluated and compared with the operating power gain of the conventional Class B power amplifier. A load network implementation with matching circuit using transmission line elements is considered with exact circuit parameters.

This article is generally complete, but is condensed from two longer papers that provide more in-depth discussion and development of the design equations and their implementations. Those papers, as well as this article, are available for downloading at this magazine's web site.

Introduction

The switched-mode Class E tuned power amplifiers with a shunt capacitance have found widespread application due to their design simplicity and high efficiency operation [1]. In the Class E power amplifier, the transistor operates as an on-off switch and the shapes of the current and voltage waveforms provide a condition where the high current and high voltage do not overlap simultaneously, to minimize the power dissipation and maximize the power amplifier efficiency. Such an operation mode can be realized for the tuned power amplifier by an appropriate choice of the values of the reactive elements in its load network [2].

However, in real practice it is impossible to realize an RF choke with infinite impedance at the fundamental and any harmonics. Moreover, using a finite DC feed inductance has an advantage of minimizing size, cost and complexity of the overall circuit. Several approaches have been proposed to analyze the effect of a finite DC feed inductance on the Class E mode with shunt capacitance [3, 4, 5]. The well-defined analytic solution based on an assumption of the even harmonic resonant conditions when the DC feed inductance and parallel capacitance are tuned on any even harmonic was published in reference [6]. Unfortunately, in this case, the optimum load resistance is over an order of magnitude smaller than for conventional Class E with shunt capacitance when an RF choke is used. As an alternative to the RF choke, a quarter wave transmission line can be used, providing simultaneously the DC current supply and suppression of even-order harmonics.

The circuit schematic with a shunt capacitance and series inductance that can provide ideally 100 percent collector efficiency is not unique. The same result can be achieved with a parallel-circuit Class E configuration [7, 8].

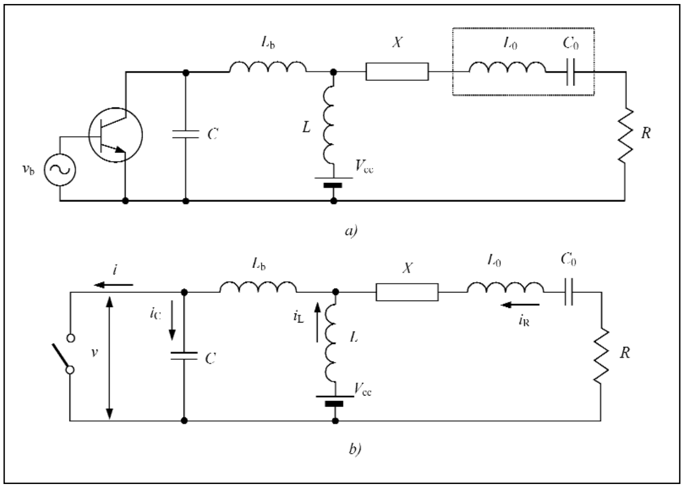


Figure 1 · Equivalent circuits of the Class E power amplifiers with generalized load network.

The basic advantage of such a load network configuration is that the parallel inductance can be used instead of RF choke and no need to use an additional series phase-shifting element.

Generalized Load Network

The generalized second-order load network of a switched-mode Class E power amplifier is shown in Figure 1(a). The load network consists of a shunt capacitance C, a series inductance L_b, a parallel inductance L, a series reactive element X and a series L_0C_0 resonant circuit tuned to the fundamental, and a load R. In a common case, a shunt capacitance C can represent the intrinsic device output capacitance and external circuit capacitance added by the load network, a series inductance L_b can be considered as a bondwire and lead inductance, a parallel inductance L represents the finite DC-feed inductance and a series reactive element X can be zero, positive (inductance) or negative (capacitance) depending on the Class E mode. The active device is considered to be an ideal switch that is driven in such a way in order to provide the device switching between its on-state and off-state operation conditions. As a result, the collector voltage waveform is determined by the transient response of the load network when the switch is off.

To simplify analysis of a general-circuit Class E power amplifier—a simple equivalent circuit of which is shown in Figure 1(b)—the following several assumptions are introduced [2]:

- The transistor has zero saturation voltage, zero saturation resistance, infinite off-state resistance and its switching action is instantaneous and lossless.
- The total parallel capacitance is independent of the collector and is assumed to be linear.
- The loaded quality factor Q_L of the series resonant L_0C_0 circuit is high enough in order the output current to be sinusoidal at the carrier frequency.
- There are no losses in the circuit except only into the load R.
- For optimum operation mode a 50% duty cycle is considered.

The characteristics of a Class E power amplifier can be determined by finding its steady-state collector voltage and current waveforms. For lossless operation mode, it is necessary to provide the following optimum conditions for voltage across the switch just prior to the start of switch on at the moment $t = 2\pi$, when transistor is saturated:

$$v(\omega t)\Big|_{\omega t=2\pi} = 0 \tag{1}$$

$$\left.\frac{dv(\omega t)}{d(\omega t)}\right|_{\omega t=2\pi} = 0 \tag{2}$$

where v is the voltage across the switch.

Expressions for the collector current ($0 \leq \omega t < \pi$) and voltage ($\pi \leq \omega t < 2\pi$) for an ideal L_0C_0 circuit tuned to the fundamental when the sinusoidal current $i_R = I_R \sin(\omega t + \varphi)$ is flowing into the load can be written by

$$\begin{aligned} i(\omega t) &= i_L(\omega t) + i_R(\omega t) \\ &= \frac{V_{cc}}{\omega(L+L_b)}\omega t + \frac{\omega L I_R}{\omega(L+L_b)}\left[\sin(\omega t+\varphi) - \sin\varphi\right] \end{aligned} \tag{3}$$

$$\omega^2(L+L_b)C\frac{d^2v(\omega t)}{d(\omega t)} + v(\omega t) - V_{cc} - \omega L I_R\cos(\omega t+\varphi) = 0 \tag{4}$$

In idealized Class E operation mode, there is no nonzero voltage and current simultaneously that means a lack of the power losses and gives an idealized collector efficiency of 100%. This implies that the DC power and fundamental output power are equal, i. e.

$$I_0V_{cc} = \frac{V_R^2}{2R} \tag{5}$$

where $V_R = I_RR$ is the voltage amplitude across the load resistance R.

Load Network with Shunt Capacitance

The basic circuit of a class E power amplifier with a shunt capacitance is shown in Figure 2 where the load network consists of a capacitance C shunting the transis-

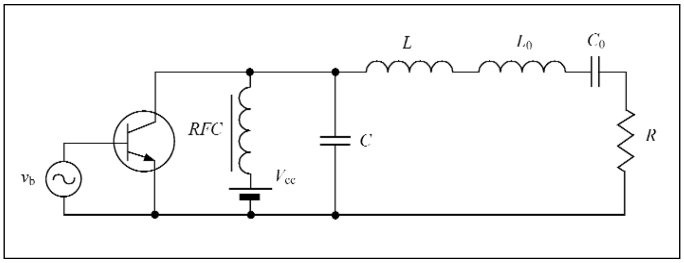


Figure 2 · Equivalent circuit of the Class E power amplifier with shunt capacitance.

tor, a series inductance L, a series fundamentally tuned L_0C_0 circuit and a load resistance R. The collector of the transistor is connected to the supply voltage by RF choke having high reactance at the fundamental frequency. Such a simplified load network represents a first-order Class E mode as their electrical behavior in time domain can be analytically described by the first-order differential equations.

The optimum series inductance L and shunt capacitance C can be found from [2]

$$L = 1.1525\frac{R}{\omega} \qquad C = \frac{0.1836}{\omega R} \tag{6}$$

whereas the optimum load resistance R can be obtained for the given supply voltage V_{cc} and output power P_{out} using

$$R = 0.5768\frac{V_{cc}^2}{P_{out}} \tag{7}$$

In Figure 3, the normalized collector voltage (a) and current (b) waveforms for idealized optimum Class E with shunt capacitance are shown. From collector voltage and current waveforms it follows that, when the transistor is turned on, there is no voltage across the switch and the current $i(\omega t)$ consisting of the load sinusoidal current i_R and DC current I_0 flows through the device. However, when the transistor is turned off, this current now flows through the shunt capacitance C.

The high Q_L assumption for the series resonant L_0C_0 circuit can lead to considerable errors if its value is actually small in practical circuits [9]. For example, for a 50% percent duty cycle the values of the circuit parameters for the loaded quality factor less than unity can differ by several tens of percents. At the same time, for $Q_L \geq 7$, the errors are found to be less than 10 percent and they becomes less than 5 percent for $Q_L \geq 10$. Also it is necessary to take into account the finite value of the RF choke inductance when it can be observed the increase of the output power for low inductance values [3, 4].

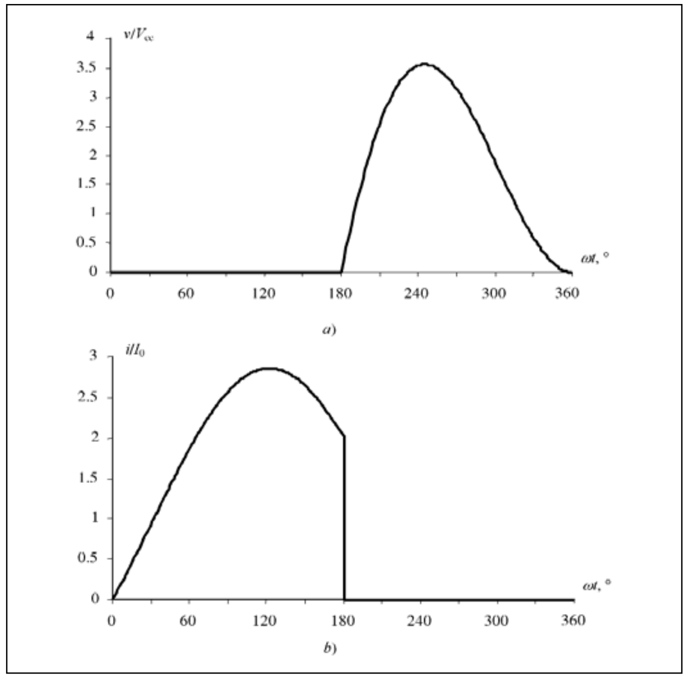


Figure 3 · Normalized collector voltage (a) and current (b) waveforms for idealized optimum Class E with shunt capacitance.

Even-Harmonic Resonant Load Network

The second-order Class E load network implies the finite value of DC feed inductance rather than ideal RF choke with infinite reactance at any harmonic components. For even harmonic Class E, the DC feed inductance is restricted to values that satisfy an even harmonic resonance condition and it is assumed that the fundamental voltage across the switch and output voltage across the load have a phase difference of $\pi/2$ [6]. Generally, even harmonic resonance condition means that the parallel inductance L and shunt capacitance C can be tuned on any even harmonic component:

$$2n = \frac{1}{\omega\sqrt{LC}} \tag{8}$$

where $n = 1, 2, 3, \ldots$.

The load network of the even harmonic Class E is shown in Figure 4 where the series capacitance C_X is needed to compensate the required phase shift. In Figure 5, the normalized collector voltage (a) and current (b) waveforms for idealized optimum even harmonic Class E mode are plotted. Although the collector voltage waveform of even harmonic Class E is very similar to the collector voltage waveform of Class E with shunt capacitance, the behavior of the current waveform is substantially different. So, for the even harmonic Class E config-

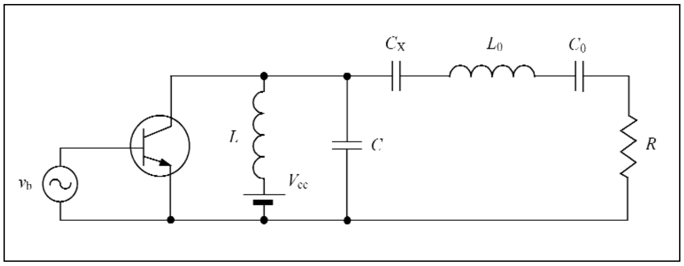


Figure 4 · Equivalent circuit of the even harmonic Class E power amplifier.

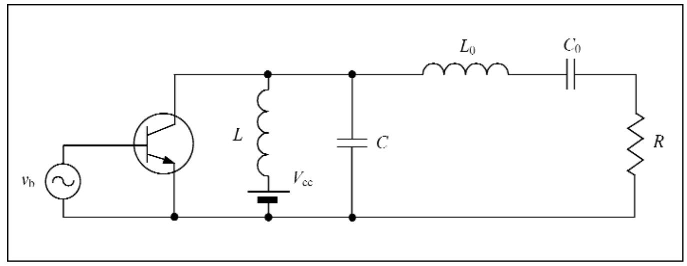


Figure 6 · Equivalent circuit of the parallel-circuit Class E power amplifier.

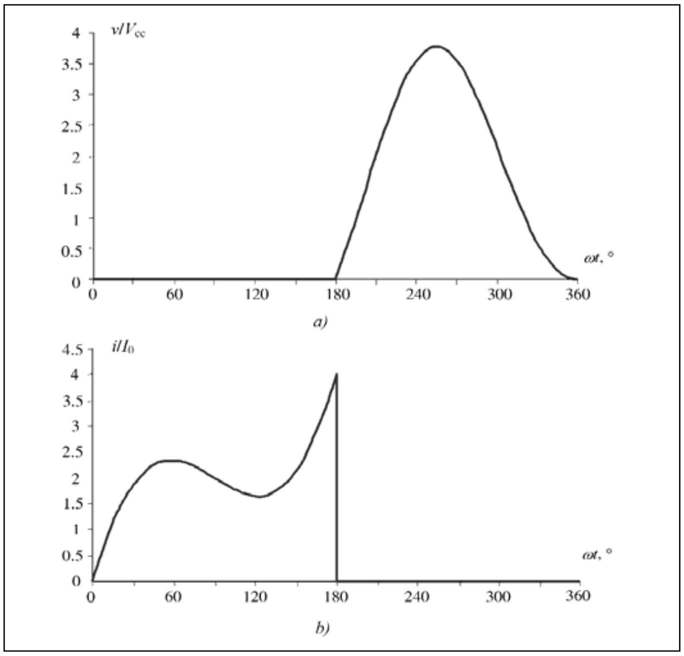


Figure 5 · Normalized collector voltage (a) and current (b) waveforms for idealized optimum even harmonic Class E.

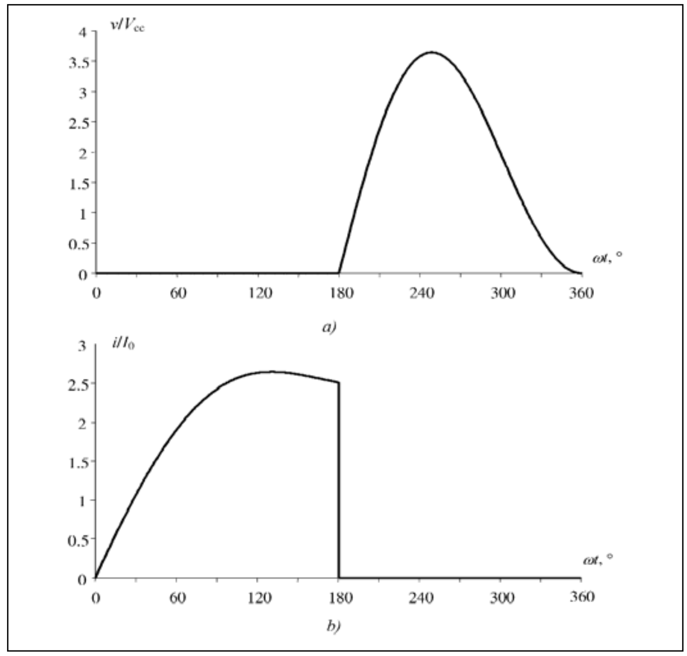


Figure 7 · Normalized collector voltage (a), and current waveforms (b) for an idealized optimum parallel-circuit Class E.

uration, the collector current reaches its peak value, which is four times greater than the DC current, at the end of the conduction interval. Consequently, in the case of the sinusoidal driving signal it is impossible to provide the maximum collector current when the input base current is smoothly reducing to zero.

The optimum load network parameters for the most practical case $n = 1$ corresponding to the second harmonic tuning can be calculated from

$$R = 0.056\frac{V_{cc}^2}{P_{out}} \qquad L = 3.534\frac{R}{\omega} \tag{9}$$

$$C = 0.071\frac{1}{\omega R} \qquad C_X = 0.204\frac{1}{\omega R} \tag{10}$$

Load Network with Parallel Circuit

The load network of a parallel-circuit Class E amplifier is shown in Figure 6. The series circuit is tuned to the fundamental frequency and the required phase shift to realize idealized voltage and current waveforms is provided by the proper choice of the three parallel circuit parameters, a parallel inductance L, a shunt capacitance C and a load resistance R. In the parallel-circuit Class E mode, no additional series phase-shifting elements are required. In Figure 7, the normalized collector voltage (a) and current (b) waveforms for idealized optimum conditions are shown.

For the parallel-circuit Class E mode, the optimum load resistance R, parallel inductance L and parallel capacitance C can be obtained, with the high Q_L assumption for the series L_0C_0 circuit [8]:

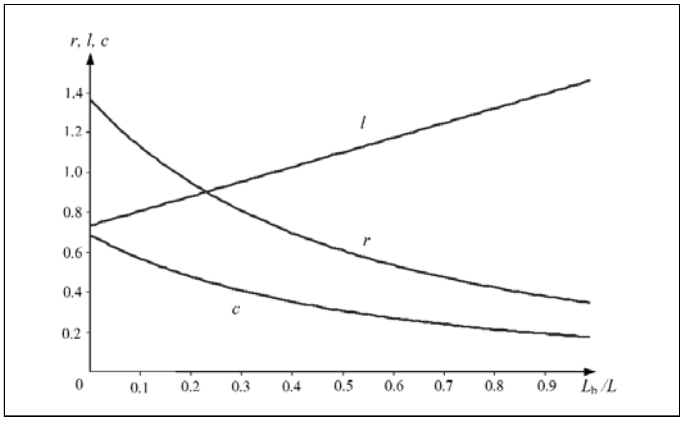


Figure 8 · Normalized optimum load network parameters versus normalized bondwire inductance L_b/L for parallel-circuit Class E.

$$R = 1.365\frac{V_{cc}^2}{P_{out}} \qquad L = 0.732\frac{R}{\omega} \qquad C = \frac{0.685}{\omega R} \tag{11}$$

Influence of Bondwire Inductance L_b

At higher frequencies when using the discrete power transistors, it is necessary to take into account the device output bondwire and lead inductance because its influence may be significant especially at high output power level and low supply voltage. The effect of bondwire inductance for even harmonic Class E configuration gives unrealistically small values for optimum load resistance and DC feed inductance when, for example, in UHF band typical values for the bondwire inductance of approximately 1 nH constitute most, if not all, of the required DC feed inductance [10].

In Figure 8, the dependences of the normalized parallel inductance $l = \omega L/R$, parallel capacitance $c = \omega CR$ and load resistance $r = RP_{out}/V_{cc}^2$ for the parallel-circuit Class E (see Figure 1 with $X = 0$) as the functions of the normalized bondwire inductance, L_b/L, are plotted. As it is shown from Figure 8, the increasing effect of the bondwire inductance L_b leads to the significantly reduced optimum values for the load resistance R and shunt capacitance C and increased optimum value for the finite DC feed inductance L.

Class E with Quarter Wave Transmission Line

The idealized Class E load network with a shunt capacitance where a quarter wave transmission line is connected between the series inductance and fundamentally tuned series L_0C_0 circuit is shown in Figure 9.

In Figure 10, the normalized collector voltage (a) and current (b) waveforms for an idealized optimum Class E mode with a quarter wave transmission line are shown.

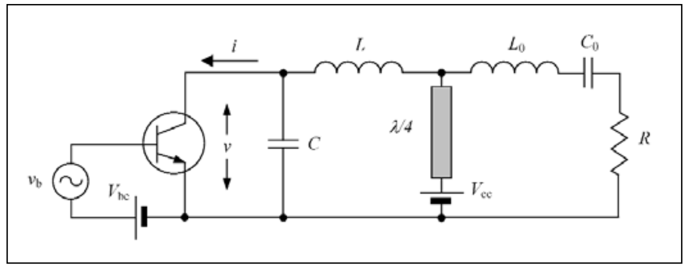


Figure 9 · Equivalent circuit of Class E power amplifier with quarter wave transmission line.

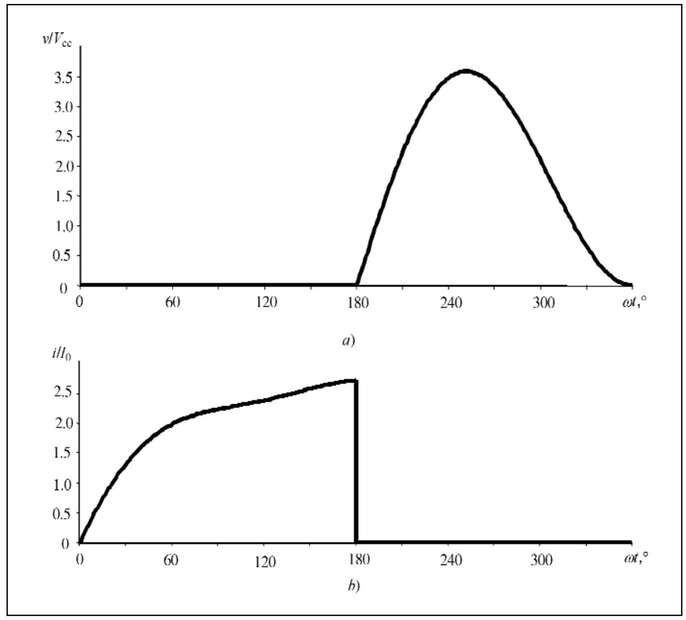


Figure 10 · Voltage and current waveforms of Class E power amplifier with quarter wave transmission line.

The series inductance L, shunt capacitance C and load resistance R with high Q_L assumption for series L_0C_0 circuit can be obtained from

$$L = 1.349\frac{R}{\omega} \qquad C = \frac{0.2725}{\omega R} \qquad R = 0.465\frac{V_{cc}^2}{P_{out}} \tag{12}$$

In Table 1, the optimum impedances seen from the device collector at the fundamental and higher-order harmonics are illustrated by the appropriate circuit configurations. It can be seen that Class E mode with a quarter wave transmission line shows different impedance properties at even and odd harmonics. At odd harmonics, the optimum impedances can be established by the shunt capacitance as it is required for all harmonics in Class E with a shunt capacitance. At even harmonics, the optimum impedances are realized using a parallel LC circuit as it is required for all harmonics in Class E with a par-

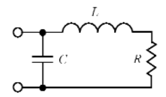
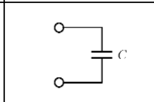
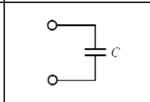
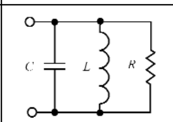
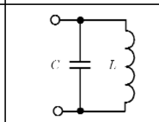
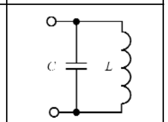
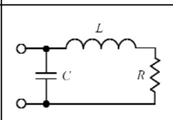
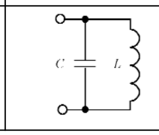
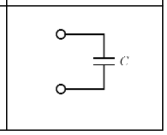
Class E load network	f_0 (fundamental)	$2nf_0$ (even harmonics)	$(2n+1)f_0$ (odd harmonics)
Class E with shunt capacitance			
Class E with parallel circuit			
Class E with quarterwave transmission line			

Table 1 · Optimum impedances at fundamental and harmonics for different Class E load networks.

allel circuit. Thus, the frequency properties of a grounded quarter wave transmission line, with its open circuit conditions at odd harmonics and short circuit conditions at even harmonics, allow Class E with a quarter wave transmission line to combine simultaneously the harmonic impedance conditions typical for both Class E with a shunt capacitance and Class E with a parallel circuit.

Matching Circuits with Lumped Elements

In practical RF circuit when impedance transformation between the load R_L and optimum resistance R is needed, the L_0C_0 filter should be replaced by the output matching circuit, which input impedance needs to be sufficiently high at second and higher-order harmonics. Generally, the lumped matching circuits in the form of an L-network, π-network or T-network can be used. However, the simplest and easiest in practical implementation matching circuit is the L-network as shown in Figure 11(a) where C_b is the blocking capacitance. Such a transformer provides the broader frequency bandwidth and enough harmonic suppression. The output matching circuit also can be designed with any combination of lumped capacitors and inductors with the series inductor as the first element in order to keep the optimum switching conditions by providing high-impedance condition at the input of matching circuit for the second and higher-order harmonics.

To calculate the circuit parameters of the L-network matching circuit, first calculate the loaded quality factor from

$$Q_L = \sqrt{\left(\frac{R_L}{R}\right) - 1} \tag{13}$$

Then, the matching circuit parameters can be determined as follows:

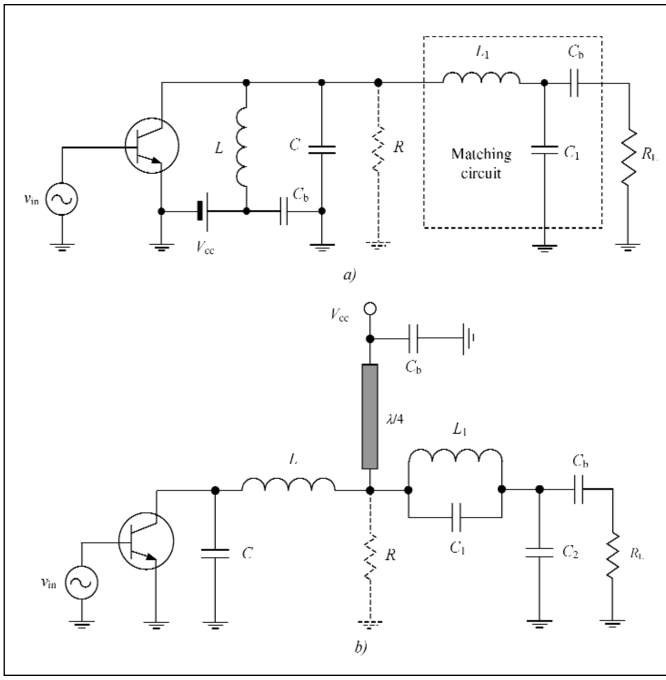


Figure 11 · Class E power amplifiers with a lumped element matching circuit.

$$C_1 = \frac{Q_L}{\omega R_L} \qquad L_1 = \frac{Q_L R}{\omega} \tag{14}$$

The theoretical results obtained for Class E mode with a quarter wave transmission line show that it is enough to use a very simple load network to realize the optimum impedance conditions even for four harmonics. In this case, the shunt capacitance C and series inductance L provide optimum inductive impedance at the fundamental and the quarter wave transmission line realizes the reduction of even harmonics. Then, an open circuit condition is required for the third harmonic component.

In Figure 11(b), the circuit schematic of the lumped Class E power amplifier with a quarter wave transmission line is shown, where the parallel L_1C_1 resonant circuit tuned on the third harmonic is used and C_b is the blocking capacitance. Since, at the fundamental the reactance of this circuit is inductive, it is enough to use the shunt capacitance C_2 to create the L-type matching circuit that provides the required impedance matching of optimum Class E load resistance R with the standard load impedance of R_L = 50 ohms.

As a result, the matching circuit parameters can be calculated from

$$C_2 = \frac{Q_L}{\omega R_L} \qquad L_1 = \frac{8}{9}\frac{Q_L R}{\omega} \qquad C_1 = \frac{1}{9\omega^2 L_1} \tag{15}$$

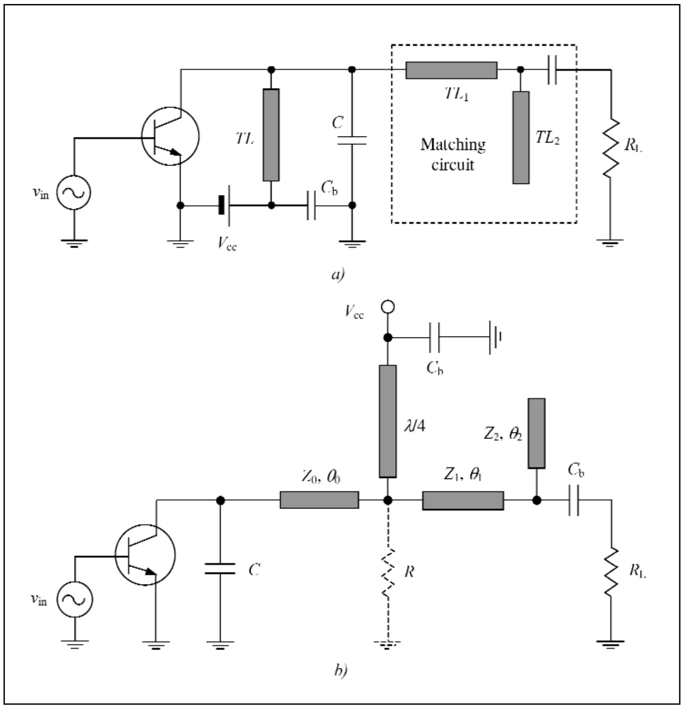


Figure 12 · Class E power amplifiers with transmission line output matching circuits.

where the loaded quality factor Q_L is defined by equation (13).

Transmission Line Matching Circuits

For a microwave power amplifier, all inductances in its load network are normally replaced by the transmission lines to reduce power losses. To approximate the idealized Class E mode, it is necessary to design the transmission line matching circuit with optimum impedance at the fundamental and provide the open circuit conditions for all harmonics. As it follows from the Fourier analysis, a good approximation to Class E mode with a shunt capacitance can be obtained with the collector voltage waveform consisting only of the fundamental and second harmonics [11]. In this case, the matching circuit contains the series microstrip line and open circuit stub with electrical lengths of about 45° at the fundamental. An additional increase of the collector efficiency can be provided by the load impedance control at the second and third harmonics simultaneously [12]. However, all these cases require an RF choke for the DC supply as a separate element.

For a parallel-circuit Class E power amplifier, the parallel inductance L at microwaves should be replaced by the short-length short-circuited transmission line TL as shown in Figure 12(a) according to

$$Z_0 \tan\theta_0 = \omega L \tag{16}$$

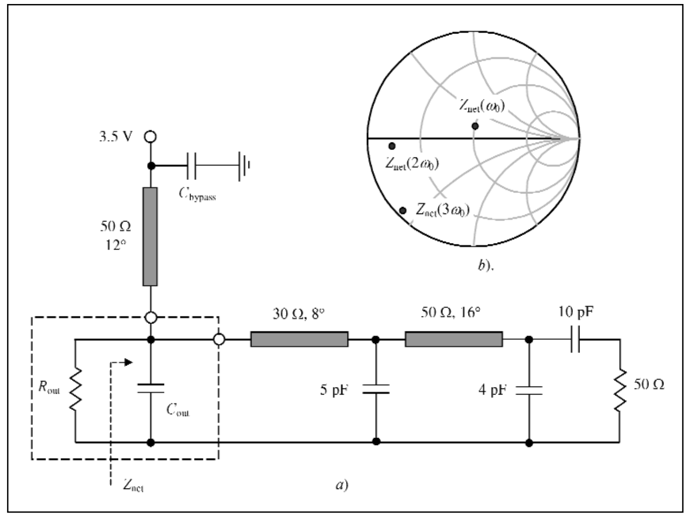


Figure 13 · Output load network of transmission line parallel-circuit Class E power amplifier for handset application.

where Z_0 and θ_0 are the characteristic impedance and electrical length of the transmission line TL, respectively [8]. The electrical lengths of the series microstrip line TL_1 and open circuit stub TL_2 are also chosen to be 45 degrees at the fundamental. To maintain the optimum switching conditions at the fundamental this matching circuit should contain the series transmission line as the first element as shown in Figure 12(a, b).

For Class E with a quarter wave transmission line, the series lumped inductance L should be replaced by the short-length series transmission line. In this case, when the shunt capacitance C represents a fully internal active device output capacitance, the bondwire and lead inductances can also be taken into account providing the required inductive reactance and making the series transmission line shorter. The circuit schematic of the transmission line Class E power amplifier with a quarter wave transmission line is shown in Figure 12(b).

As the transmission line characteristic impedance Z_0 is normally much higher than the optimum resistance R, the optimum value of θ_0 for Class E mode is obtained by

$$\theta_0 = \tan^{-1}\left(1.349\frac{R}{Z_0}\right) \tag{17}$$

The output matching circuit is necessary to match the required optimum resistance R to a 50-ohm load and provide an open circuit condition at the third harmonic. The electrical lengths of the series line and open circuit stub are chosen equal to 30 degrees each. The conjugate matching with the load is provided when the characteristic impedances Z_1 and Z_2 are calculated from

$$\frac{Z_1}{R_L} = \frac{\sqrt{4r-3}}{r} \qquad \frac{Z_1}{Z_2} = 3\left(\frac{r-1}{r}\right) \tag{18}$$

where $r = R_L/R$, R_L = 50 ohms and the optimum load resistance R is calculated using equation (12).

Another possible transmission line circuit configuration is shown in Figure 13(a). This circuit was developed for a monolithic handset power amplifier and includes the series transmission line with parallel capacitances [13]. However, because of the finite electrical length of the transmission lines (not a quarter wave length) it is impossible to simultaneously realize the required inductive impedance at the fundamental frequency with pure capacitive reactances at higher-order harmonics. Even at the second harmonic the real part of the circuit input impedance is quite high as shown in Figure 13(b). Nevertheless, such an approach allows the design of power amplifiers with extremely high efficiency and a good approximation to the parallel-circuit Class E operation mode. In this case, there is no need to use an additional RF choke for the DC supply, as this function can be performed by a very short parallel microstrip line. The practical design procedure consists of two steps: first, to provide the required (or close to the required if the device output capacitance exceeds the optimum value) inductive impedance at the fundamental using the parallel transmission line (equivalent of a parallel inductance L) and shunt capacitance C; and secondly, to realize conjugate matching of the 50-ohm load with the optimum load resistance R required for parallel-circuit Class E mode for a given output power and supply voltage. The final results can then be verified with the simulated collector voltage and current waveforms.

Power Gain

In order to realize the idealized switching conditions, the load network of any type of Class E mode is mistuned at the fundamental frequency, thus violating the conjugate matching conditions required for conventional Class B operation. This means that the output voltage and current waves consist of both incident and reflected components. However, the load impedance conditions for Class E mode differ from those for Class B mode. The operating power gain G_P expressed through the active device Y-parameters and load can be obtained by

$$G_P = \frac{|Y_{21}|^2}{\mathrm{Re}\,Y_{\mathrm{in}}} \frac{R}{|Y_{22}+Y_L|^2} \tag{19}$$

where Y_{21}, Y_{22} are the device Y-parameters, Y_{in} is the device input admittance and $Y_L = G + jB$ is the load admittance, while $R = 1/G$ is the load resistance [14].

By substituting the real and imaginary parts of the device Y-parameters and load admittance, the ratio between the operating power gain of the switched-mode Class E power amplifier $G_{P(E)}$ and the operating power gain of the conventional Class B power amplifier $G_{P(B)}$ with conjugate-matched load can be written by

$$\frac{G_{P(E)}}{G_{P(B)}} = \frac{1}{1+\left(B_{22}+B\right)^2 R_{(E)}^2} \frac{R_{(E)}}{R_{(B)}} \tag{20}$$

where $R_{(E)}$ is the optimum load resistance of the Class E power amplifier and $R_{(B)}$ is the optimum load resistance of the Class B power amplifier.

As a result, for ideal 100-percent efficiency parallel-circuit Class E operation mode, for the same output power P_{out} and taking into account that in conventional Class B with zero saturation voltage $V_{R(B)} = V_{cc}$, the power gain ratio can be obtained by

$$\frac{G_{P(E)}}{G_{P(B)}} = \frac{1}{1+\tan^2\phi} \frac{R_{(E)}}{R_{(B)}} = 1.865 \tag{21}$$

where

$$\frac{R_{(E)}}{R_{(B)}} = \frac{V_{R(E)}^2}{V_{R(B)}^2} = 2.729$$

and ϕ = 34.244° is the phase angle between the fundamental-frequency voltage and current across the switch required for the optimum switched-mode operation [8].

The result given by equation (21) means that, ideally, the operating power gain for the switched-mode parallel-circuit Class E mode compared with conventional Class B mode is practically the same and even slightly greater despite the mistuning of the output load network. This can be explained by the larger value of the load required for the optimum Class E mode. The idealized conditions for switched-mode operation can be achieved with instant on-off active device switching, which requires the rectangular input driving signal compared with sinusoidal driving signal for conventional Class B mode. However, the power losses due to the switching time are sufficiently small and, for example, for switching time of τ_s = 0.35 or 20° are only of about 1% [8, 14]. Consequently, a slight overdrive the active device is needed when the input power should be increased by 1-2 dB to minimize switching time and maximize the collector efficiency of the switched-mode Class E power amplifier. As a result, the resulting power gain becomes approximately equal to the power gain of the conventional Class B power amplifier.

References

1. N. O. Sokal, and A. D. Sokal, "Class E - A New Class of High-Efficiency Tuned Single-Ended Switching Power Amplifiers," *IEEE J. Solid-State Circuits*, Vol. SC-10, pp. 168-176, June 1975.

2. F. H. Raab, "Idealized Operation of the Class E Tuned Power Amplifier," *IEEE Trans. Circuits and Systems*, Vol. CAS-24, pp. 725-735, Dec. 1977.

3. R. E. Zulinski, and J. W. Steadman, "Class E Power Amplifiers and Frequency Multipliers with Finite DC-Feed Inductance," *IEEE Trans. Circuits and Systems*, Vol. CAS-34, pp. 1074-1087, Sept. 1987.

4. C. P. Avratoglou, N. C. Voulgaris, and F. I. Ioannidou, "Analysis and Design of a Generalized Class E Tuned Power Amplifier," *IEEE Trans. Circuits and Systems*, Vol. CAS-36, pp. 1068-1079, Aug. 1989.

5. G. H. Smith, and R. E. Zulinski, "An Exact Analysis of Class E Power Amplifiers with Finite DC-Feed Inductance at Any Output Q," *IEEE Trans. Circuits and Systems*, Vol. CAS-37, pp. 530-534, April 1990.

6. M. Iwadare, S. Mori, and K. Ikeda, "Even Harmonic Resonant Class E Tuned Power Amplifier without RF Choke," *Electronics and Communications in Japan*, Vol. 79, pp. 23-30, Jan. 1996.

7. A. V. Grebennikov, and H. Jaeger, "Class E with Parallel Circuit — A New Challenge for High-Efficiency RF and Microwave Power Amplifiers," *2002 IEEE MTT-S Int. Microwave Symp. Digest,* Vol. 3. pp. 1627-1630.

8. A. V. Grebennikov, "Switched-Mode RF and Microwave Parallel-Circuit Class E Power Amplifiers," *Int. J. RF and Microwave Computer-Aided Eng.*, Vol. 14, Jan. 2004.

9. M. Kazimierczuk, and K. Puczko, "Exact Analysis of Class E Tuned Power Amplifier at any Q and Switch Duty Cycle," *IEEE Trans. Circuits and Systems*, Vol. CAS-34, pp. 149-158, Feb. 1987.

10. D. K. Choi, *High Efficiency Switched-Mode Power Amplifiers for Wireless Communications*, Ph.D. Dissertation, University of California, Santa Barbara, March 2001.

11. T. B. Mader, E. W. Bryerton, M. Marcovic, M. Forman, and Z. Popovic, "Switched-Mode High-Efficiency Microwave Power Amplifiers in a Free-Space Power-Combiner Array," *IEEE Trans. Microwave Theory Tech.*, Vol. MTT-46, pp. 1391-1398, Oct. 1998.

12. F. J. Ortega-Gonzalez, J. L. Jimenez-Martin, A. Asensio-Lopez, and G. Torregrosa-Penalva, "High-Efficiency Load-Pull Harmonic Controlled Class-E Power Amplifier," *IEEE Microwave and Guided Wave Lett.*, Vol. 8, pp. 348-350, Oct. 1998.

13. H. Jaeger, A. V. Grebennikov, E. P. Heaney, and R. Weigel, "Broadband High-Efficiency Monolithic InGaP/GaAs HBT Power Amplifiers for Wireless Applications," *Int. J. RF and Microwave Computer-Aided Eng.*, Vol. 13, pp. 496-510, Nov. 2003.

14. H. L. Krauss, C.W. Bostian, and F. H. Raab, *Solid State Radio Engineering*, Wiley, 1980.

Author Information

Andrei Grebennikov received his MSc degree in electronics from Moscow Institute of Physics and Technology and PhD degree in radio engineering from Moscow Technical University of Communications and Informatics in 1980 and 1991, respectively. He joined the scientific and research department of the Moscow Technical University of Communications and Informatics as a research assistant in 1983. His scientific and research interests include the design and development of power RF and microwave radio transmitters for base station and handset applications, hybrid integrated circuits and MMICs of high-efficiency and linear microwave and RF power amplifiers, single-frequency and voltage-controlled oscillators using any type of bipolar and field-effect transistors. From 1998 to 2001, Grebennikov was a member of technical staff at the Institute of Microelectronics, Singapore, responsible for the design and development LDMOSFET high power amplifier modules. Since January 2001 he has been with the M/A-COM Eurotec (Cork, Ireland) where he is involved in the design and development of 3G handset InGaP/GaAs HBT power amplifier modules. He can be reached by email at: grandrei@ieee.org

Expanded Papers are Available Online at:
www.highfrequencyelectronics.com

The author has provided two papers with expanded discussions of these topics, which are available online at this magazine's web site:

www.highfrequencyelectronics.com

Until mid-September 2004, the links to "Exact Time-Domain Analysis of Class E Power Amplifiers with Quarter wave Transmission Line" and "Load Network Design Technique for Switched-Mode Tuned Class E Power Amplifiers" can be found in the Table of Contents for the July 2004 issue.

After that time, the papers will be included with the contents of the July 2004 issue in the "Archives" section of the site. Just click on "Article Archives" from the main web page and scroll down to the desired issue.